Amendments to the SUBSTITUTE Specification

Please replace the paragraph beginning on page 4, line 20 with the following amended paragraph:

The column selecting pulse generator 10 generates a column selecting pulse YCLK in response to a clock signal CLK and a burst signal BURST. The burst signal BURST has a "H" level during a column accessing operation. The write clock generator 11 generates a signal WDE in response to the column selecting pulse YCLK and a signal WRITE. The signal WRITE has the "H" level while a write operation. The data bus equalizing signal generator 12 generates an equalizing signal DBEQ in response to the column selecting signal YCLK. The write driver & data bus equalizer unit 13 transfers an input data to the data bus in response to the signal WDE and equalizes the data bus in response to the equalizing signal DBEQ. The ~~pre-decoder~~ pre-decoders 14 ~~pre-decodes~~ include pre-decoders 14A, 14B, 14C and 14D that respectively pre-decode address signal A0 to A8 and respectively generate ~~generates~~ pre-decode signals PY0_1_2[0:7], PY3_4[0:3], PY5_6[0:3], and PY7_8[0:3], hereinafter referred to as signals PY0, PY1, PY2, PY3, PY4, PY5, PY6, PY7 and PY8, or collectively for the sake of brevity as PY0 – PY8 [[PY]]. In this embodiment, the lower three bits (A0 to A2) are used for selecting the memory cell blocks 19 and another six bit (A3 to A8) are used for selecting the column selecting lines Y. In a burst access operation, lower address A0 alternately changes between the "H" and the "L" levels for every column accessing. Therefore, when the column lines are selected sequentially,

two consecutive column accessing operations are performed in two respective memory cell blocks 19. The address drivers ~~driver~~ 15 ~~outputs~~ output the pre-decode signals [[PY]] PY0 – PY8 to the column decoder 16 in synchronization with the column selecting pulse YCLK. The column decoder 16 outputs block selecting signals YBSEL[0:7] and the column selecting signals Y[0:63] in response to the pre-decode signals PY0 – PY8 [[PY]]. The row decoder & main word line driver unit 17 outputs array selecting signals XASEL[0:3] in response to an array selecting signal ASEL[0:3] and the burst signal BURST.

Please replace the paragraph beginning on page 8, line 6 with the following amended paragraph:

First, the memory cell array is selected by the array selecting signal XASEL[0:3]. Then, the block selecting signal YBSEL[k] and the column selecting signal Y[i] are changed to the "H" level in synchronization with the column selecting pulse YCLK which is generated from the clock signal CLK and the burst signal BURST, wherein YBSEL [k] is indicative of an asserted one of block selecting signals YBSEK[0] to YBSEL[7], and Y[i] is indicative of a corresponding asserted one of column selecting signals Y[0] to Y[63] initially selected for a writing operation. Then, the transistors 222 and 223 are turned on and the data bus DB and DBb are connected to the sense amplifier 301 in response to the "H" level of the column selecting signal Y[i]. The gate signals TGR and TGL are changed to the "L" level in response to the block selecting signal YBSEL, and

the sense amplifier 301 is disconnected from the bit line pair BL[i] and BLb[i] by the transfer gates 302 and 303. In Fig. 4, gate signals TGR and TGL are collectively shown as TGR(L) for the sake of brevity, because the pair of signals TGR and TGL provided by a given control block 111 as shown in Fig. 3 have the same values simultaneously responsive to the corresponding block selecting signal YBSEL. That is, data is transferred from the data bus DB and DBb to the input nodes SBL and SBLb of the sense amplifier 301 while the sense amplifier 301 is disconnected from the bit line pair BL[i] and BLb[i]. As a result, the level of the input node SBL of the sense amplifier 301 is changed to the "L" level and the level of the input node SBLb of the sense amplifier 301 is changed to the "H" level immediately.

Please replace the paragraph beginning on page 9, line 2 with the following amended paragraph:

In response to the "H" level of the block selecting signal YBSEL[I] and the column selecting signal Y[j], wherein YBSEL[I] is indicative of a next asserted one of block selecting signals YBSEL[0] to YBSEL[7], and Y[j] is indicative of a corresponding next asserted one of column selecting signals Y[0] to Y[63] selected for a next writing operation, another sense amplifier 301 in another memory cell block 19 starts latching next data. The another sense amplifier 301 is connected to a bit line pair BL[j] and BLb[j] that is selected by the block selecting signal YBSEL[I] and the column selecting signal Y[j]. The latching operation in the another sense amplifier 301 is started while

the writing operation from the sense amplifier 301 to the bit line pair BL[i] and BLb[i] is performed. The memory cell block 19 is selected by the lower address A0 to A2. Therefore, the bit line pair BL[i] and BLb[i] which is selected by the column selecting signal Y[i] and the bit line pair BL[j] and BLb[j] which is selected by the column selecting signal Y[j] are included in the different memory cell blocks respectively. As a result, the data latching operation in the sense amplifier 301 which is connected to the bit line pair BL[j] and BLb[j] which is selected by the column selecting signal Y[j] can be performed while the writing operation for the bit line pair BL[i] and BLb[i] which is selected by the column selecting signal Y[i] is performed.

Please replace the paragraph beginning on page 11, line 2 with the following amended paragraph:

Next, a writing operation is described by referring to Fig. 7, which shows among other signals a clock signal CLK having clock cycle tCYC.